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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/630,983	07/30/2003	Hideharu Koike	500-002	7730
24002	7590	08/11/2004	EXAMINER	
ANTHONY R BARKUME 20 GATEWAY LANE MANORVILLE, NY 11949			NGUYEN, HAI L	
			ART UNIT	PAPER NUMBER
			2816	

DATE MAILED: 08/11/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

in

Office Action Summary

Application No.

10/630,983

Applicant(s)

KOIKE, HIDEHARU

Examiner

Hai L. Nguyen

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 30 July 2003.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-14 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-14 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 30 July 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☒ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 7 and 12 are rejected under 35 U.S.C. 102(b) as being anticipated by Konno (US 5,914,516).

With regard to claim 7, Konno discloses in Fig. 3 an integrated circuit comprising a transition circuit (by given the broadest reasonable interpretation; elements 11, 12, 13 is the transition circuit because it has a function of transferring signal from input to the output), the input of the transition circuit being coupled with an input pad (1) of the integrated circuit, the output of the transition circuit being coupled with an input buffer (2); a first capacitor (14) being inserted between the output of the transition circuit and a first voltage source (4); and a second capacitor (15) being inserted between the output of the transition circuit and a second voltage source (7).

With regard to claim 12, the reference also meets the recited limitation in this claim.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

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(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1-3, 5, and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gans et al. (US 6,353,521) in view of Konno.

With regard to claim 1, Gans et al. discloses in Fig. 2 an integrated circuit comprising a CMOS inverter (5), the input of the CMOS inverter being coupled with an input pad (25) of the integrated circuit, the output of the CMOS inverter being coupled with an input buffer (51). Fig. 2 of Gans et al. shows a circuit meeting all of the claimed limitations, except for a first capacitor (212 in instant Fig.2) being inserted between the output of the CMOS inverter and a first voltage source; and a second capacitor (213) being inserted between the output of the CMOS inverter and a second voltage source, note that it also means the first and second capacitors being inserted between the input (N1) of the input buffer (14) and the first and second voltage sources, respectively. Konno teaches in Fig.3 a circuit having a first capacitor (14) being inserted between the input (3) of the input buffer (2) and a first voltage source (4) and a second capacitor (15) being inserted between the input of the input buffer and a second voltage source (7) as recited in the claim. Therefore, it would have been obvious to one of ordinary skill in the art to implement those capacitor taught by Konno with the prior art (Fig. 2 of Gans et al.) in order to improve the surge protection function.

With regard to claims 2 and 3, the above discussed circuit of the references meets all of the claimed limitations except for Gans et al. does not disclose that the integrated circuit is a LSI or a VLSI. However, it would have been obvious to one of ordinary skill in the art to realize that any integrated circuit (many types of which are well known in the

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art including a LSI or a VLSI as recited in the claims) can benefit from the circuit taught by the references for the advantage of being able to improve the surge protection function of the integrated circuit. Therefore, the claimed invention does not define patentably over the circuitry of the references.

With regard to claims 5 and 6, the references also meet the recited limitations in these claims.

5. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gans et al. in view of Konno, as applied to claim 1 above, and further in view of the admitted prior art, Fig. 1 in the present application.

With regard to claim 4, the above-discussed circuit of the references meets all of the claimed limitations except that the buffer circuit (51 in Fig. 2 of Gans et al.) is not a Schmitt-trigger type buffer circuit. The admitted prior art (Fig. 1 in the present application) shows a circuit having a Schmitt trigger (14) as a buffer circuit. Since the admitted prior art and the circuit of the references are similar, it would have been obvious to one of ordinary skill in the art at the time of applicant's invention was made utilize a Schmitt trigger circuit as the buffer circuit (51 in Fig. 2 of Gans et al.) in the references' circuit in order to remove any noise spikes around the threshold point of its input on both the rising and falling edges of the input signal.

6. Claims 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Konno.

With regard to claims 8 and 9, the above discussed circuit of the references meets all of the claimed limitations except for Konno does not disclose that the integrated circuit is a LSI or a VLSI. However, it would have been obvious to one of ordinary skill

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in the art to realize that any integrated circuit (many types of which are well known in the art including a LSI or a VLSI as recited in the claims) can benefit from the circuit taught by the references for the advantage of being able to improve the surge protection function of the integrated circuit. Therefore, the claimed invention does not define patentably over the circuitry of the references.

7. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Konno in view of the admitted prior art, Fig. 1 in the present application.

With regard to claim 11, the above-discussed circuit of the references meets all of the claimed limitations except that the buffer circuit (2 in Fig. 3 of Konno) is not a Schmitt-trigger type buffer circuit. The admitted prior art (Fig. 1 in the present application) shows a circuit having a Schmitt-trigger (14) as a buffer circuit. Since the admitted prior art and the circuit of the references are similar, it would have been obvious to one of ordinary skill in the art at the time of applicant's invention was made utilize a Schmitt trigger circuit as the buffer circuit (2 in Fig. 3 of Konno) in the reference's circuit in order to remove any noise spikes around the threshold point of its input on both the rising and falling edges of the input signal.

8. Claims 7-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Singh (US 6,069,515) in view of Konno.

With regard to claim 7, Singh discloses in Figs. 1-3 an integrated circuit comprising a transition circuit (102, 104, 106, 300, 302, 304, 306; Fig. 3), the input of the transition circuit being coupled with an input pad (100) of the integrated circuit, the output of the transition circuit being coupled with an input buffer (110, 112, 114; Fig. 2). Figs. 1-3 of Singh show the circuit meeting all of the claimed limitations, except for a

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first capacitor (212 in instant Fig.2) being inserted between the output of the transition circuit and a first voltage source; and a second capacitor (213) being inserted between the output of the transition circuit and a second voltage source, note that it also means the first and second capacitors being inserted between the input (N1) of the input buffer (14) and the first and second voltage sources, respectively. Konno teaches in Fig.3 a circuit having a first capacitor (14) being inserted between the input (3) of the input buffer (2) and a first voltage source (4) and a second capacitor (15) being inserted between the input of the input buffer and a second voltage source (7) as recited in the claim. Therefore, it would have been obvious to one of ordinary skill in the art to implement those capacitor taught by Konno with the prior art (Figs. 1-3 of Singh) in order to improve the surge protection function.

With regard to claims 8 and 9, the above discussed circuit of the references meets all of the claimed limitations except for Singh does not disclose that the integrated circuit is a LSI or a VLSI. However, it would have been obvious to one of ordinary skill in the art to realize that any integrated circuit (many types of which are well known in the art including a LSI or a VLSI as recited in the claims) can benefit from the circuit taught by the references for the advantage of being able to improve the surge protection function of the integrated circuit. Therefore, the claimed invention does not define patentably over the circuitry of the references.

With regard to claim 10, the transition circuit includes two transfer gates, the two transfer gates are a NMOS transistor (102) and a PMOS transistor (103).

Claim 11 is rejected for similar motivation; note the above discussion with regard to claims 4 and 1.

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With regard to claim 12, the first voltage source is VDD (3.3V).

With regard to claim 13, a reference voltage (1.1V to 2.2V) of the transition circuit is VDD/2.

With regard to claim 14, the second voltage source is VSS.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. For example, Chiang (US 5,329,174) is cited as of interest because it discloses a circuit for forcing known voltage on unconnected pads of an integrated circuit.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hai L. Nguyen whose telephone number is 571-272-1747 and Right Fax number is 571-273-1747. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The official fax phone number for the organization where this application or proceeding is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 571-272-1562.

HLN 
August 8, 2004


TIMOTHY P. CALLAHAN
SUPERVISORY PATENT EXAMINER
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